DESIGN AND IMPLEMENTATION OF REAL-TIME UNDERWATER ACOUSTIC TRANSCEIVER USING DIGITAL SIGNAL PROCESSORS

Fu-Sheng Lu1, Ching-Hsiang Tseng2, and Bin-Chong Wu2

|  |  |
| --- | --- |
| 1Department of Computer and Communication Engineering, St. John's University, Taipei County, Taiwan, R.O.C.  E-mail: [lufs@mail.sju.edu.tw](mailto:lufs@mail.sju.edu.tw) | 2Department of Electrical Engineering, National Taiwan Ocean University, Keelung, Taiwan, R.O.C.  E-mail: [lmfs@mail.sju.edu.tw](mailto:lmfs@mail.sju.edu.tw) |
|  |  |

Abstract

In this paper, an all-digital transceiver for real-time underwater acoustic (UWA) communications is developed using digital signal processors (dsps). The design of the transceiver is based on the direct-sequence spread-spectrum (DS/SS) modulation scheme, in which the timing synchronization is efficiently achieved by employing a sliding correlator and a modified noncoherent delay-locked loop for code acquisition and tracking, respectively. In addition, an equal-gain combiner (EGC) and an adaptive decision-feedback equalizer (DFE) are included in the receiver to enhance its interference rejection capability under multipath fading environments. Several real-time UWA transmission tests are conducted in an experimental water tank to evaluate the performance of the transceiver. The test data include plain text and simple image files. The test result shows that reliable real-time UWA communications can be accomplished by the proposed transceiver.

**Key words**: underwater acoustic communication, direct-sequence spread spectrum, delay-locked loop, synchronization.

# INTRODUCTION

The UWA communication channel is generally considered as an unfavorable and difficult environment for data transmission. Its multipath fading and Doppler spreading effects make the building of a reliable UWA communication system a challenging task. Most commercially available UWA communication systems developed so far use noncoherent modulation schemes like the frequency shift keying (FSK) for simplicity. However, as the hardware technology progresses, the focus of the UWA communication research has been shifted toward more complicated coherent modulation schemes such as phase shift keying (PSK) and quadrature amplitude modulation (QAM) [3, 8]. Furthermore, the design of UWA transceivers has been revolutionized over the past few years due to the tremendous advances in DSP technology [2, 4, 9, 12]. The digital VLSI offers communication engineers a platform to realize algorithms that were frequently inconceivable in the analog domain. Specifically, Choi et al. [1, 2] presented a design of phase-coherent all-digital UWA transceiver whose frame synchronization method requires neither a phase-locked loop (PLL) nor a delay-locked loop (DLL), and the operation of the transceiver relies largely on the adaptive equalizer and the Viterbi decoding algorithm. Trubuil et al. [9] developed a real-time high data rate UWA communication link, where a self-optimized configuration multiple input decision feedback equalizer (SOC-MI-DFE) was proposed and implemented on a TMS320 C6201 DSP module. These all-digital implementations require the sampling of the received signal to be synchronized to the incoming symbols. Interpolation methods for achieving such synchronization have also been proposed by several researchers [5, 11].

# THE TRANSCEIVER STRUCTURE

## 2.1 Transmitter

The bit stream to be transmitted is organized in frames as shown in Figure 1. The preamble and the end code indicate the start and the end of a message frame, respectively. They are used by the receiver for the frame synchronization. The training sequence is used by the adaptive equalizer in the receiver for optimizing the equalizer coefficients. The information-bearing data follow the training sequence. The gap between the preamble and the training sequence is for ensuring the completion of the frame synchronization in the receiver before the reception of the training sequence.



Figure 1. The frame structure of the transmitted bit stream.

The block diagram of the transmitter is illustrated in Figure 2. The channel encoder employs the BCH code. The multiplexer adds the preamble, the training sequence, and the end code to the information bearing data to form a bit stream with the frame format shown in Figure 1. The DS/SS modulator performs the QPSK modulation on the incoming bit stream and then multiplies the modulated signal with the spreading signal generated by a pseudo-random noise (PN) code generator. The digital-to-analog converter (DAC) converts the digital DS/SS signal to an analog signal. This signal, after being boosted by the power amplifier, is then passed to the UWA channel through the hydrophone.



Figure 2. Block diagram of the transmitter.

# PROCESSING TECHNIQUES

## 3.1 Synchronization Schemes

The purpose of timing synchronization is to allow the locally generated spreading signal to synchronize with the one embedded in the received signal. The timing synchronization is usually achieved in two stages: code acquisition and code tracking. The code acquisition is used to bring the timing offset between the received signal and the locally generated spreading signal to within the pull-in range of the code tracking loop, and then the code tracking can be initiated to correct the timing offset.

The control circuit adjusts the timing alignment between the locally generated spreading signal and the received signal. When the timing alignment is correct, the correlator output will reach its maximal value. Therefore, the code acquisition can be attained by examining the peak locations of the correlator output signal.

The code tracking process can be accomplished by using a noncoherent DLL [6]. In this paper, we introduce a modified noncoherent DLL which is slightly different from the conventional one. In the modified version, the local spreading signal generator provides only one specific signal, and the received signal is shifted to yield the early and the late signals. The displacements of the shifting are controlled by the voltage-controlled oscillator (VCO). This process can be conducted by using the intrinsic registers of the DSP module and therefore can be easily implemented.

The operation of the modified noncoherent DLL is explained as follows. Suppose that the baseband signal at the transmitting end is denoted by , then  can be expressed as

 (1)

where  is the *k*th data bit, is the impulse response of the pulse shaping filter at the transmitter, and  is the bit duration.

Table 1. Comparison of bit error rates for the simulation.

|  |  |  |  |
| --- | --- | --- | --- |
| number of receivers | without equalization | with equalization | with BCH code |
| 1 |  |  |  |
| 2 |  |  |  |

## 3.2 Adaptive Equalization

Equalization can compensate for the ISI resulting from the multipath fading effects of UWA channels. Several researchers have proposed various adaptive equalizers in their developments of underwater communication systems [2, 9, 13]. In this paper, we employ a simple DD-DFE for its effectiveness in diminishing the ISI caused by multipath fading effects of UWA channels [13].

## 3.3 Diversity

Diversity techniques, which are widely used for combating multipath fading effects, can be implemented in many ways. In this paper, we adopt a relatively simple yet effective spatial diversity technique called equal gain combining (EGC). The EGC combines the received signals from multiple hydrophones at different spatial locations to form a signal with a higher signal-to-noise ratio (SNR).

# SIMULATION

To test the effectiveness of the proposed transceiver under fading environments, we conducted a simulation using a five-ray Rayleigh fading channel model [7]. In this simulation, we utilized a DS/SS QPSK modulation with a 7-bit PN code. A (15, 11) BCH error correction code was employed. The carrier frequency was 24 kHz, the sampling rate was 384 kHz, the symbol rate was 1985 symbols/sec, and the SNR was set to 9 dB. The simulation result is shown in Table 1. The result for using two receivers with the EGC technique is also shown in Table 1. We see the EGC technique does improve the BER performance.

# IMPLEMENTATION

Two Texas Instruments TMS320 C6711 DSK modules [10], together with an ADC and a DAC, are used to build up the proposed all-digital transceiver. The integrated circuit chips AD7891-1 and DAC8462 of Analog Devices are used as the ADC and the DAC, respectively, in the transceiver. In the transmitter program, either a plain text file or a simple image file is read and then converted to binary to form a bit stream. This bit stream, after being encoded with a (7,4) BCH code, is further divided into frames. The preamble, the training sequence, and the end code are added to each frame according to Fig. 1. Once a frame is ready, the transmitter program enables the internal interrupt function of the transmitter DSK module and then waits for the interrupt. To improve the computational efficiency of the subprogram, the sample values of the QPSK waveforms are pre-calculated and stored as a table in the transmitter DSK module for fast accessing. The current sample value of the selected waveform is sent to the DAC for generating the corresponding analog waveform before the transmitter subprogram ends. The rate of the interrupt (i.e., the sampling rate) can be controlled by setting the value of the timer period register. After the transmitter interrupt subprogram is done with transmitting a sample, the transmitter main program checks whether the end of a frame is reached. If not, the main program will proceed to process the next sample by going back to wait for the interrupt, otherwise the main program will disable the DSK internal interrupt and start processing the next frame. The main program will end when all of the data frames are processed.

The receiver program first enables the internal interrupt of the receiver DSK module and then waits for the interrupt. An interrupt will start the receiver interrupt subprogram. The receiver interrupt subprogram enables the ADC and lets the ADC sample the received signal. After the receiver subprogram ends, the receiver main program will check to see if the data buffer is full. If not, the receiver main program will go back to wait for the next interrupt, otherwise it will disable the internal interrupt of the receiver DSK module. A frame of data is resolved from the data buffer via the succeeding frame synchronization, code synchronization, de-spreading, equalizing, and BCH decoding processes. For enhancing the computational efficiency of the program, the sample values of the spreading signal required by the receiver are stored in the register for fast accessing. After the frame of data is retrieved, the main program is ready for processing the next frame of data and will go back to enable the internal interrupt unless the end of data is reached. Once the end of data is reached, the receiver main program will display the received data on the computer screen.

# EXPERIMENTS

To evaluate the goodness of the designed transceiver, transmitting and receiving experiments were conducted in the Underwater Communications Laboratory at National Taiwan Ocean University (NTOU). At the transmitter end, a B&K 2713 power amplifier was used to magnify the transmitted signal waveform, and a B&K 8103 hydrophone was used as a sound transmitter (projector). At the receiving end, three B&K 8104 hydrophones were employed as a wide-range measuring transducer, and the signals received by the hydrophones were filtered and boosted by a B&K 2635 charge amplifier. Note that the water tank is not an anechoic tank. Its glassy surfaces yield strong reverberations which cause severe multipath fading effects.

Due to the strong reverberations of the water tank, the intersymbol interference is in fact the dominating impairment of water tank channel. We found that increasing the power level of the transmitted signal could not significantly improve the system performance. Therefore, the power and noise levels are not specified in our experiments.

In all of the experiments, the carrier frequency is 18.750 kHz, the sampling rate is 150 kHz, the frame length is 224 bits/frame, and the data rate is 1,210 bits/sec. Since the QPSK modulation is adopted, the symbol rate is 605 symbols/sec. We used different PN codes for the preamble and the data. The spreading code for the preamble is a 32-bit PN sequence, while the one for the data is a 31-bit PN sequence.

# Conclusion

Unlike terrestrial wireless communications in which data is transmitted by means of the electromagnetic wave, underwater communications use the acoustic wave instead. The propagation characteristics of the acoustic wave create a challenging environment for establishing reliable data transmissions. In this paper, an all-digital real-time UWA transceiver is proposed. The main contribution of this paper is that it integrates many state-of-the-art digital communications and signal processing techniques into one working UWA transceiver, efficiently implements the transceiver on DSK modules, and successfully tests the implementation in real-time data transmissions over an experimental UWA channel. Specifically, the DS/SS, the EGC diversity, the DD-DFE equalization, and the BCH channel coding techniques are utilized by the transceiver to achieve effective communications through the UWA channel. The proposed transceiver is implemented on two TMS320 C6711 DSK modules, one as the transmitter and the other as the receiver. The implementation for the transceiver is simple yet effective. The goodness of the implemented transmitter is tested by real-time data transmissions through an experimental water tank mimicking the actual UWA channel. The test result indicates that, although the water tank suffers from severe reverberations, reliable data transmissions can still be accomplished by the proposed transceiver.

References

1. Choi, Y., Kim, S.-M., Park, J.-W., Lim, Y.-K., and Ko, H.-L., “A digital acoustic transceiver for underwater communication without PLL and DLL,” *Proceeding of IEEE Oceans Conference*, Vol. 4, pp. 1781-1785 (2003).
2. Choi, Y., Park, J.-W., Kim, S.-M., and Lim, Y.-K., “A phase coherent all-digital transmitter and receiver for underwater acoustic communication systems,” *Proceeding of the 35th Southeastern Symposium on System Theory*, pp. 79-83 (2003).
3. Kilfoyle, D. B. and Baggeroer, A. B., “The state of the art in underwater acoustic telemetry,” *IEEE Journal of Oceanic Engineering*, Vol. 25, No. 1, pp. 4-27 (2000).
4. Labat, J., “Real time underwater communications,” *Proceeding of IEEE Oceans Conference*, Vol. 3, pp. 501-506 (1994).
5. Lu, F.-S., Tseng, C.-H., Chen, L.-W., Chen, C.-C., and Wu, B.-C., ”A design of synchronization and equalization subsystems for an all-digital underwater pager,” (in Chinese), *Proceeding of the Sixth Conference on UnderSea Technology* , pp. 81-90 (2004).
6. Peterson, R. L., Ziemer, R. E., and Borth, D. E., *Introduction to Spread-Spectrum Communication*, Prentice Hall (1995).
7. Rappaport, T. S., *Wireless Communications Principles and Practice*, *2nd Ed*., Prentice-Hall (2002).
8. Stojanovic, M., “Recent advances in high-speed underwater acoustic communications,” *IEEE Journal of Oceanic Engineering*, Vol. 21, No. 2, pp. 125-136 (1996).
9. Trubuil, J., Le Gall, T., Lapierre, G., and Labat, J., “Development of a real-time high data rate acoustic link,” *Proceeding of IEEE Oceans Conference and Exhibition*, Vol. 4, pp. 2159-2164 (2001).
10. Tseng, C.-H., Lu, F.-S., Chen, F.-K., and Wu, S.-T., ”Compensation on multi-path fading in underwater spread-spectrum communication systems,” *Proceeding of IEEE International Symposium on Underwater Technology*, pp. 453-458 (1998).
11. Vesma, J. and Saramaki, T., “Interpolation filters with arbitrary frequency response for all-digital receivers,” *Proceeding of IEEE International Symposium on Circuits and Systems*, Vol. 2, pp. 568 -571 (1996).
12. Yagnamurthy, N. K. and Jelinek, H. J., “A DSP based underwater communication solution,” *Proceeding of IEEE Oceans Conference*, Vol. 1, pp. 120 – 123 (2003).
13. Yang, T. C., “Differences between passive-phase conjugation and decision-feedback equalizer for underwater acoustic communications,” *IEEE Journal of Oceanic Engineering*, Vol. 29, No. 2, pp. 472-487 (2004).